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# DESCRIPTION

PT6311 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52-pin plastic QFP Package. Twelve segment output lines, 8 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6311 via a three-line serial interface.

# FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (12 x 4 matrix)
- Multiple Display Modes: (12 segments, 16 digits to 20 segments, 8 digits)
- 8-Step Dimming Circuitry
- LED Ports Provide (5 channels, 20mA max.)
- 4- Bits General Purpose Input Ports Provided
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 52pins QFP and LQFP

# APPLICATION

- Microcomputer Peripheral Devices

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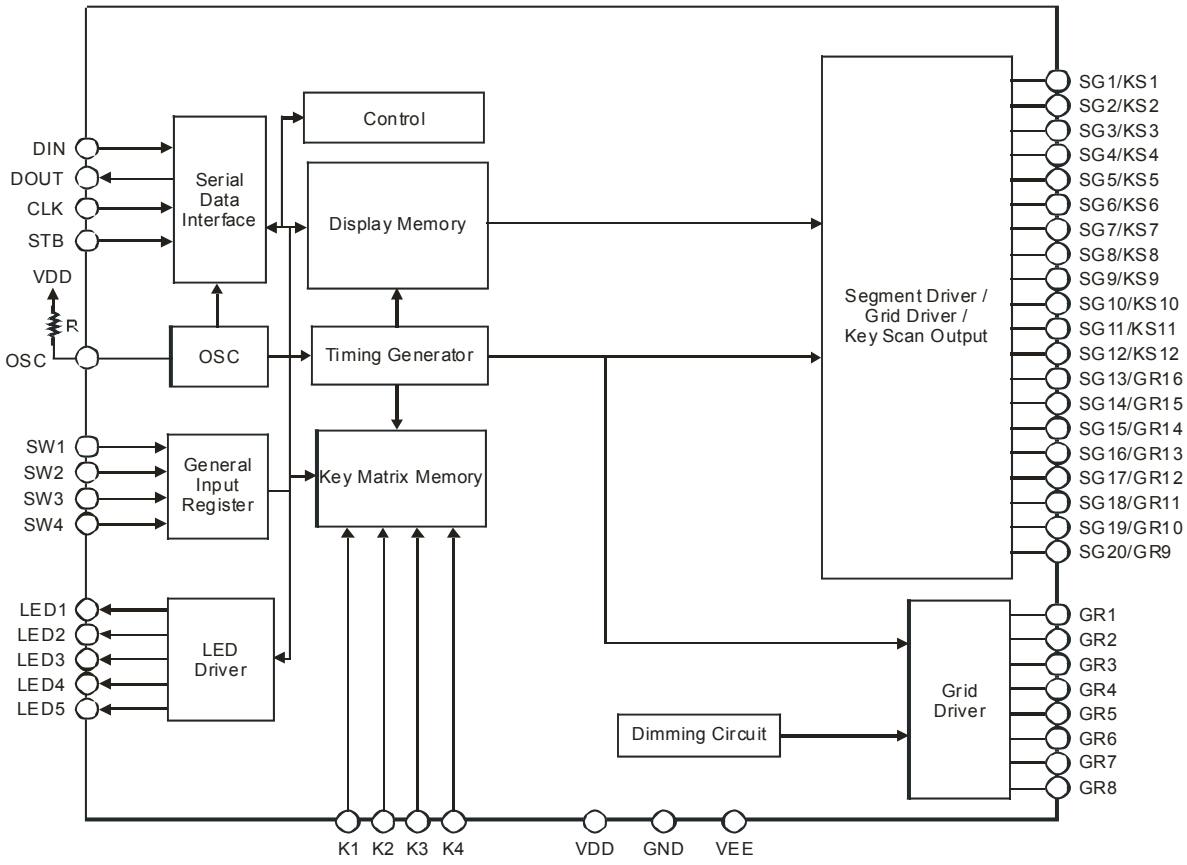
# BLOCK DIAGRAM



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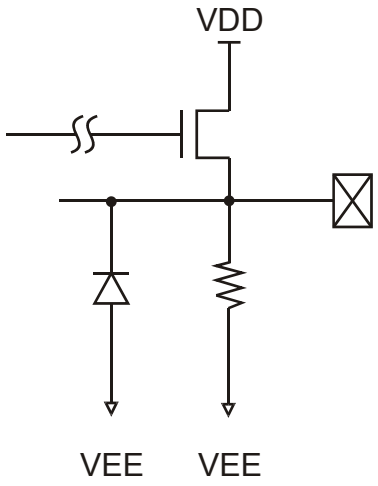
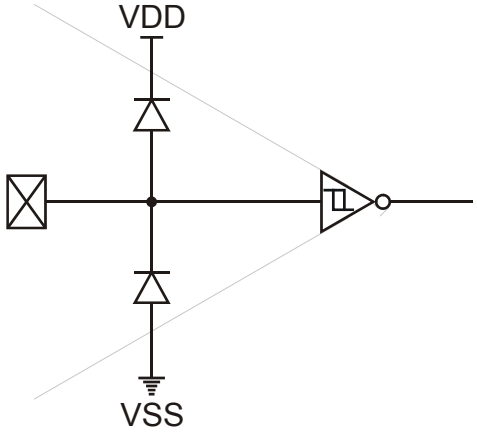
# INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

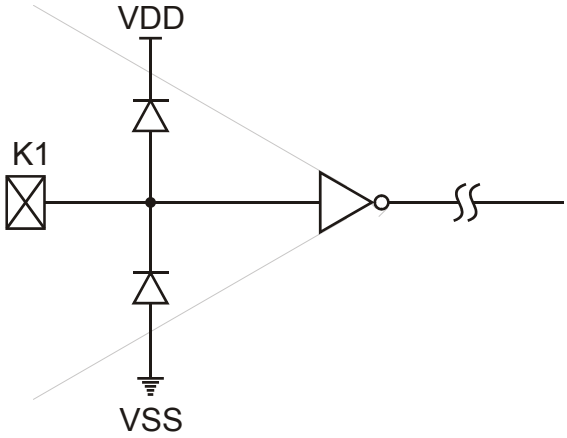
**Output Pins: SGn/GRn**




**INPUT PINS: DIN, CLK, STB**




**Input Pins: SW1 to SW4, K1 to K4**



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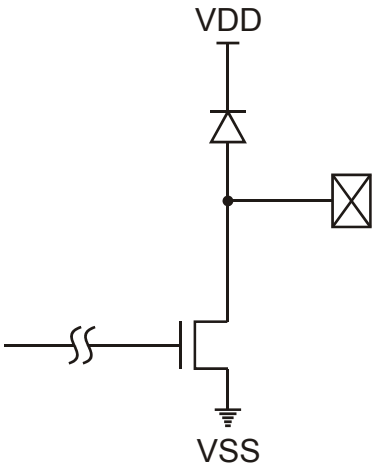
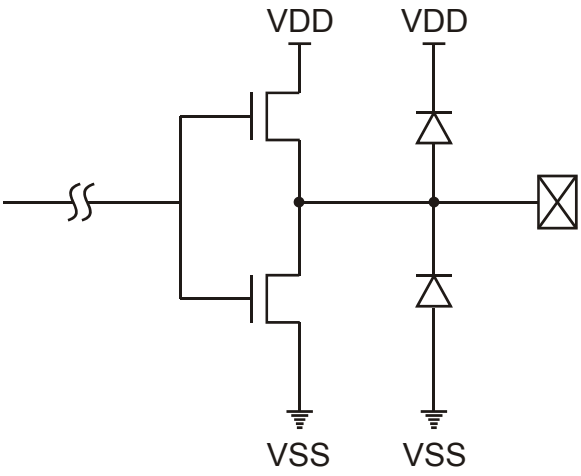
## OUTPUT PIN: DOUT




## OUTPUT PINS: LED1 TO LED5



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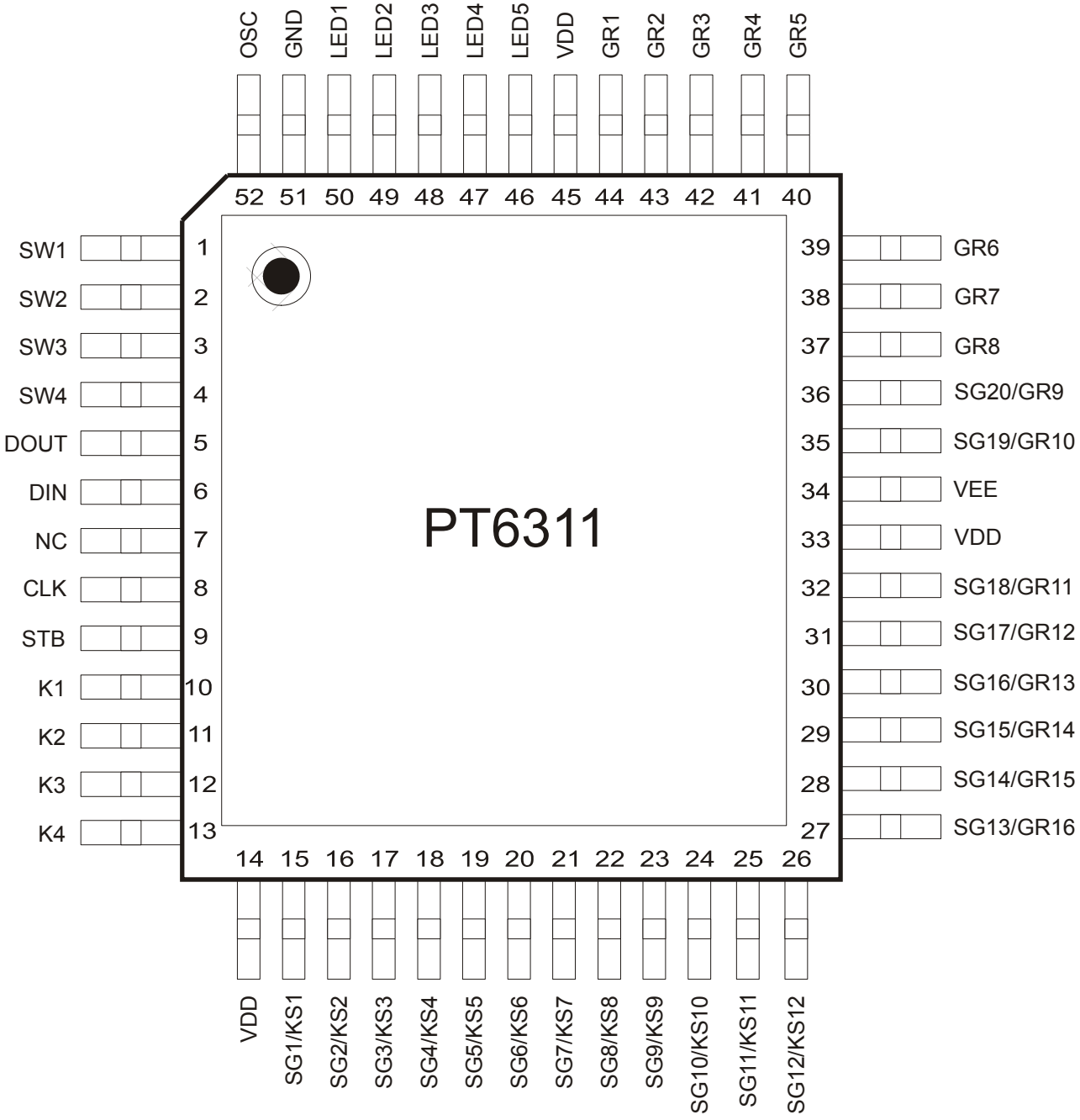
# PIN CONFIGURATION



# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| SW1 to SW4 | I | General Purpose Input Pins | 1 to 4 |
| DOUT | O | Data Output Pin (N-Channel, Open-Drain)<br>This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit). | 5 |
| DIN | I | Data Input Pin<br>This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit). | 6 |
| NC | - | No Connection | 7 |
| CLK | I | Clock Input Pin<br>This pin reads serial data at the rising edge and outputs data at the falling edge. | 8 |
| STB | I | Serial Interface Strobe Pin<br>The data input after the STB has fallen is processed as a command. When this in is "HIGH", CLK is ignored. | 9 |
| K1 to K4 | I | Key Data Input Pins<br>The data inputted to these pins is latched at the end of the display cycle. | 10 to 13 |
| VDD | - | Logic Power Supply | 14, 33, 45 |
| SG1/KS1 to SG12/KS12 | O | High-Voltage Segment Output Pins<br>Also acts as the Key Source. | 15 to 26 |
| SG20/GR9 to SG19/GR10<br>SG18/GR11 to SG13/GR16 | O | High-Voltage Segment/Grid Output Pins | 36 to 35<br>32 to 27 |
| VEE | - | Pull-Down Level | 34 |
| GR1 to GR8 | O | High-Voltage Grid Output Pins | 44 to 37 |
| LED1 to LED5 | O | LED Output Pin | 50 to 46 |
| GND | - | Ground Pin | 51 |
| OSC | I | Oscillator Input Pin<br>A resistor is connected to this pin to determine the oscillation frequency. | 52 |

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# FUNCTION DESCRIPTION

## *COMMANDS*

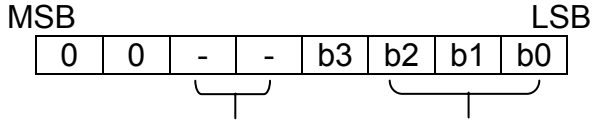
Commands determine the display mode and status of PT6311. A command is the first byte (b0 to b7) inputted to PT6311 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

## COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6311 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6311 via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 20 to 12 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 16-digit, 12-segment modes is selected.




Not Relevant

Display Mode Settings:
0XXX: 8 digits, 20 segments
1000: 9 digits, 19 segments
1001: 10 digits, 18 segments
1010: 11 digits, 17 segments
1011: 12 digits, 16 segments
1100: 13 digits, 15 segments
1101: 14 digits, 14 segments
1110: 15 digits, 13 segments
1111: 16 digits, 12 segments

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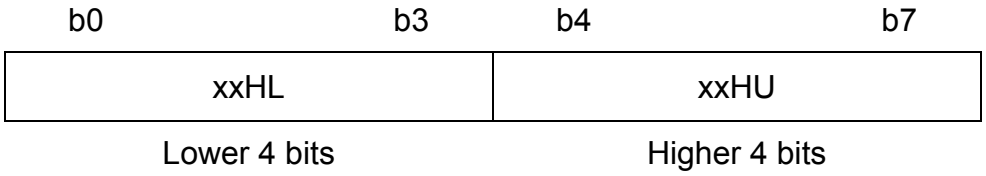
**Display Mode and RAM Address**

Data transmitted from an external device to PT6311 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6311 are given below in 8 bits unit.

| SG1 | SG4 | SG5 | SG8 | SG9 | SG12 | SG13 | SG16 | SG17 | SG20 | |
|---|---|---|---|---|---|---|---|---|---|---|
| 00HL | | 00HU | | 01HL | | 01HU | | 02HL | | DIG1 |
| 03HL | | 03HU | | 04HL | | 04HU | | 05HL | | DIG2 |
| 06HL | | 06HU | | 07HL | | 07HU | | 08HL | | DIG3 |
| 09HL | | 09HU | | 0AHL | | 0AHU | | 0BHL | | DIG4 |
| 0CHL | | 0CHU | | 0DHL | | 0DHU | | 0EHL | | DIG5 |
| 0FHL | | 0FHU | | 10HL | | 10HU | | 11HL | | DIG6 |
| 12HL | | 12HU | | 13HL | | 13HU | | 14HL | | DIG7 |
| 15HL | | 15HU | | 16HL | | 16HU | | 17HL | | DIG8 |
| 18HL | | 18HU | | 19HL | | 19HU | | 1AHL | | DIG9 |
| 1BHL | | 1BHU | | 1CHL | | 1CHU | | 1DHL | | DIG10 |
| 1EHL | | 1EHU | | 1FHL | | 1FHU | | 20HL | | DIG11 |
| 21HL | | 21HU | | 22HL | | 22HU | | 23HL | | DIG12 |
| 24HL | | 24HU | | 25HL | | 25HU | | 26HL | | DIG13 |
| 27HL | | 27HU | | 28HL | | 28HU | | 29HL | | DIG14 |
| 2AHL | | 2AHU | | 2BHL | | 2BHU | | 2CHL | | DIG15 |
| 2DHL | | 2DHU | | 2EHL | | 2EHU | | 2FHL | | DIG16 |



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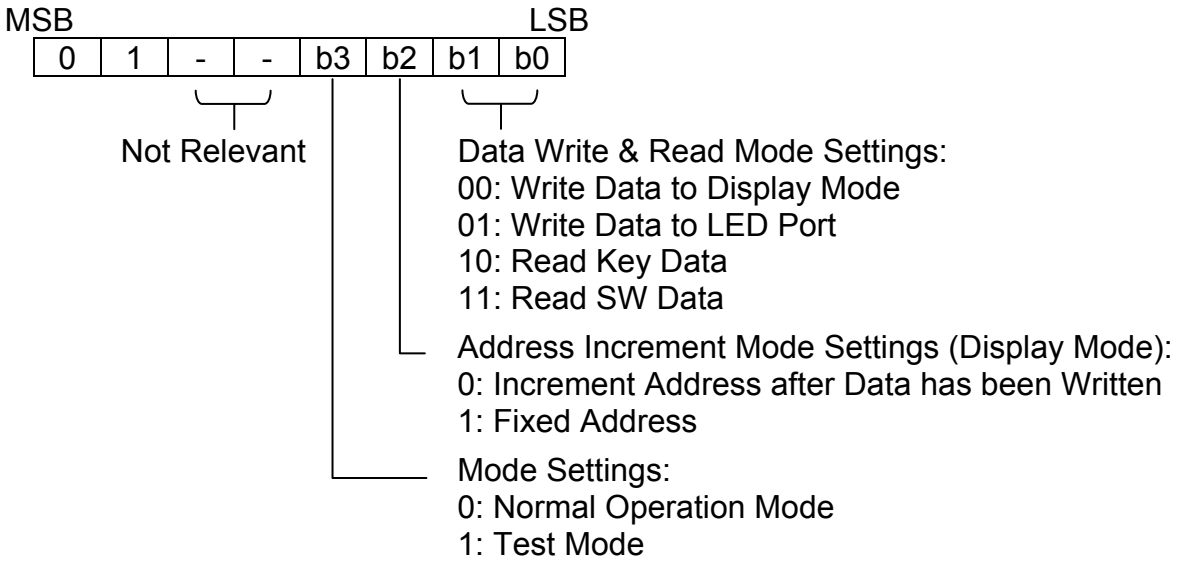
## COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6311. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "0".



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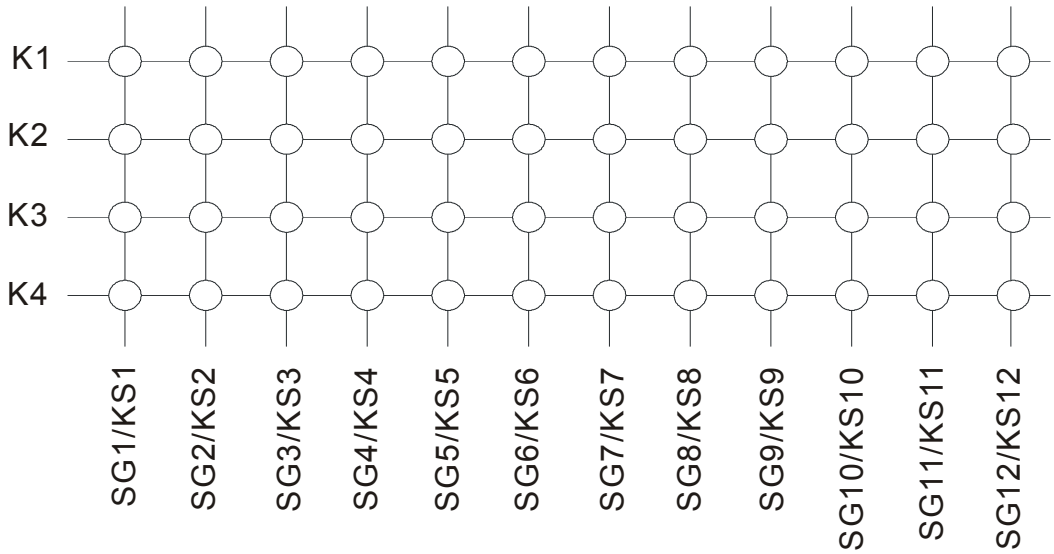
**PT6311 Key Matrix & Key Input Data Storage RAM**

PT6311 Key Matrix consists of 12 x 4 array as shown below:




Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG12, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

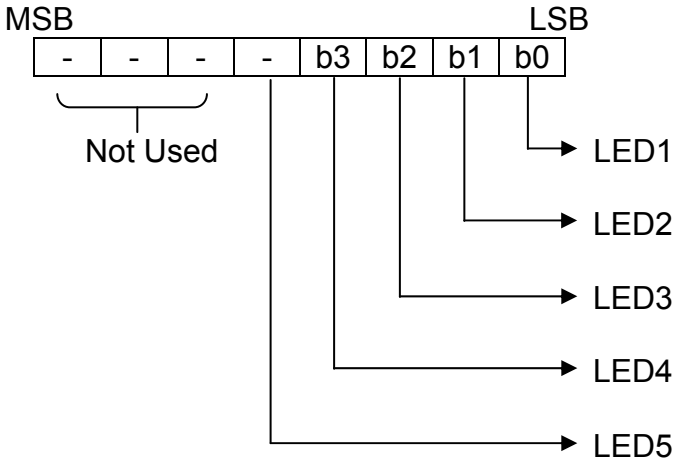
| K1……K4 | K1……K4 |
|---|---|
| SG1/KS1 | SG2/KS2 |
| SG3/KS3 | SG4/KS4 |
| SG5/KS5 | SG6/KS6 |
| SG7/KS7 | SG8/KS8 |
| SG9/KS9 | SG10/KS10 |
| SG11/KS11 | SG12/KS12 |
| b0……b3 | b4……b7 |

Reading Sequence

**LED Display**

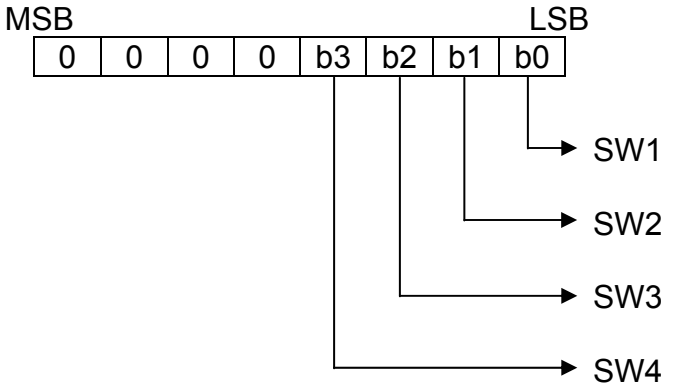
PT6311 provides 5 LED Display Terminals, namely LED1 to LED5. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 5 LED display terminals, bits 6 to 8 (b5 ~ b7) are not used and therefore ignored. This means that b5 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

When a bit (b0 ~ b4) in the LED Port is "0", the corresponding LED is ON. Conversely, when the bit is "1", the LED Display is turned OFF. For example, Bit 1 (as designated by b0) has the value of "0", then this means that LED1 is ON. It must be noted that when power is turned ON, bit 5 to bit 1 (b4 to b0) are given the value of "1". Please refer to the diagrams below:




**Switch Data**

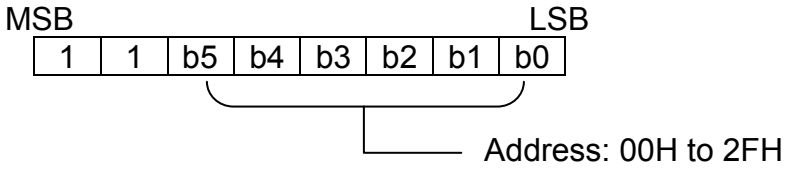
PT6311 provides 4 Switch Inputs, namely: SW1 to SW4. SW Data is read starting from the least significant bit (b0) using a READ Command. Each bit starting from the least significant (b0) corresponds to a specific Switch Input -- b0 corresponds SW1, b1 to SW2 and so forth. Since there are only 4 Switch Inputs, Bits 5 to 8 (b4 to 7) are given the value of "0". Please refer to the diagram below.



## COMMAND 3: ADDRESS SETTING COMMANDS

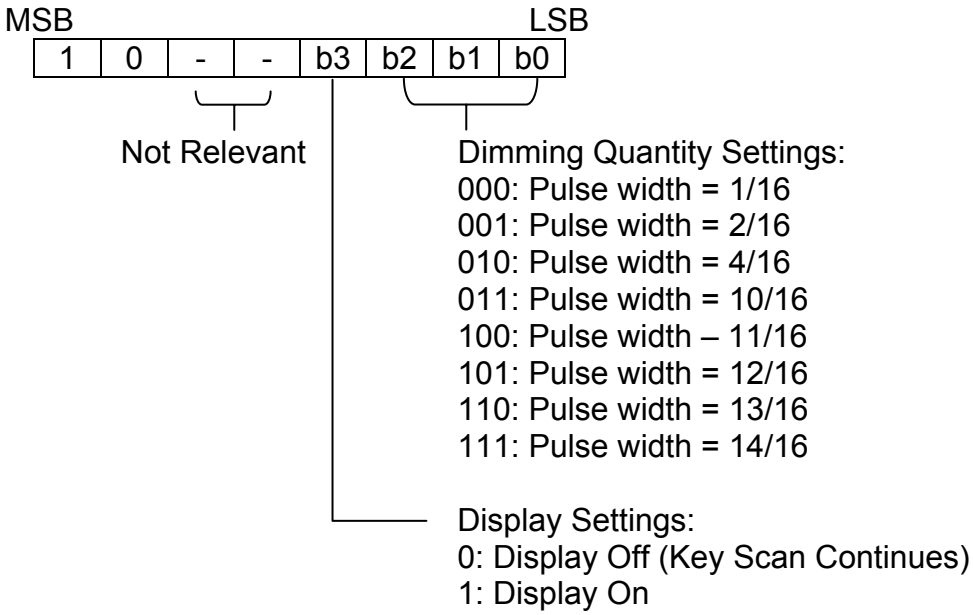
Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to “2FH”. If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



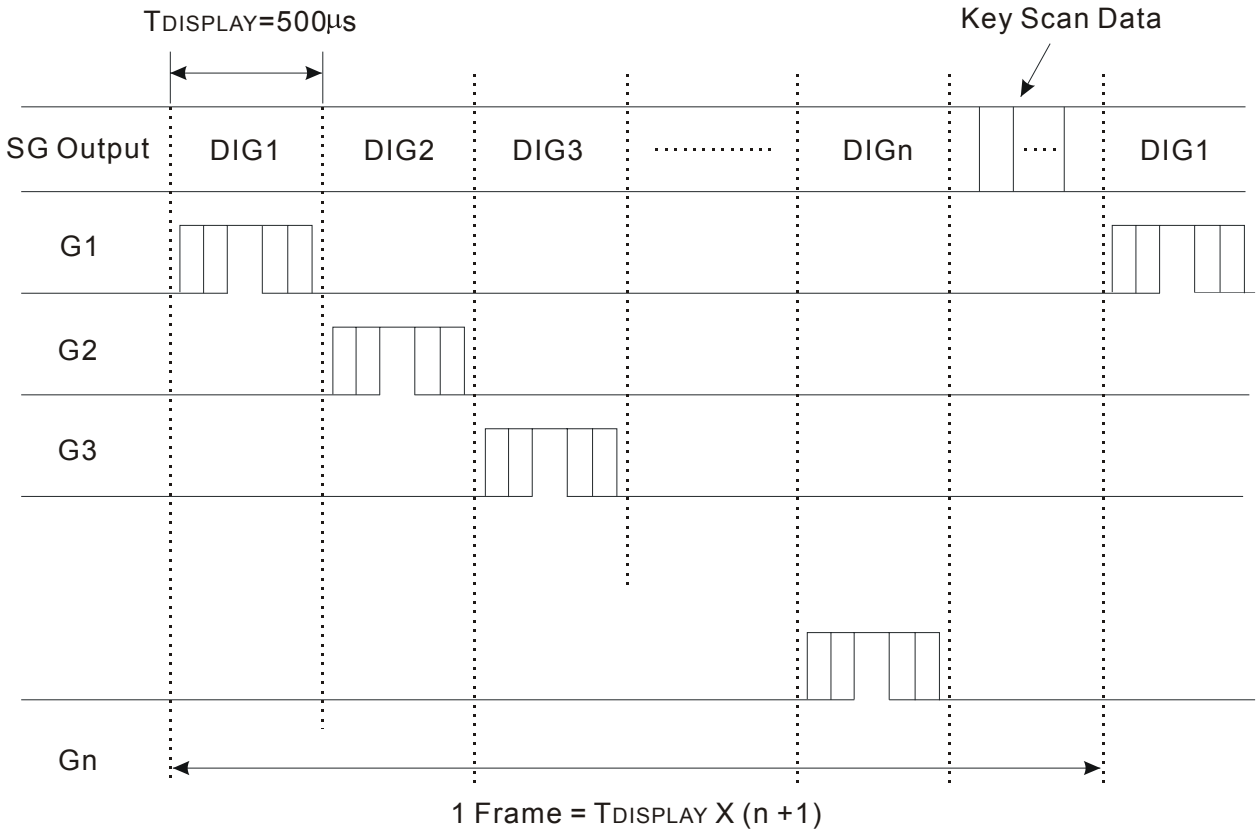

## COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).



# SCANNING AND DISPLAY TIMING

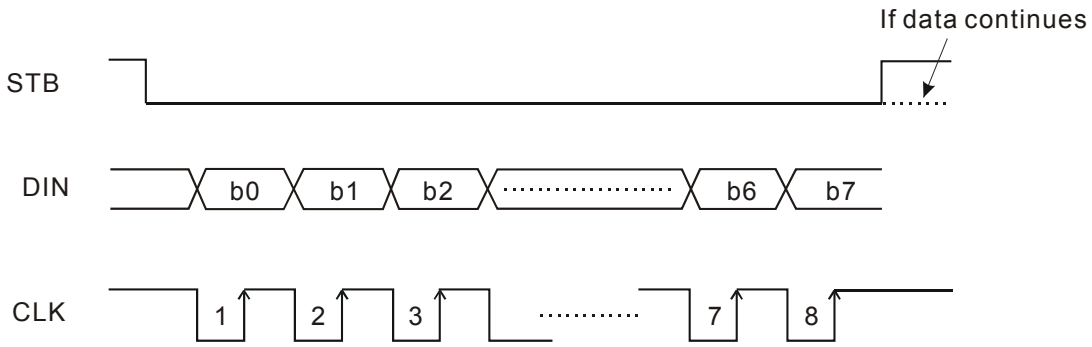
The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the are 12 x 4 matrix is stored in the RAM.



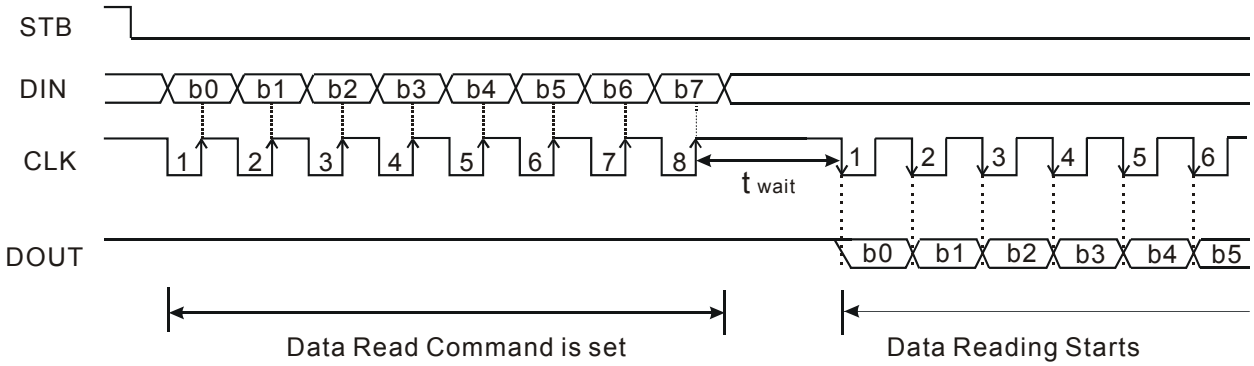
# SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6311 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

## Reception (Data/Command Write)




## Transmission (Data Read)




where: twait (waiting time) > 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

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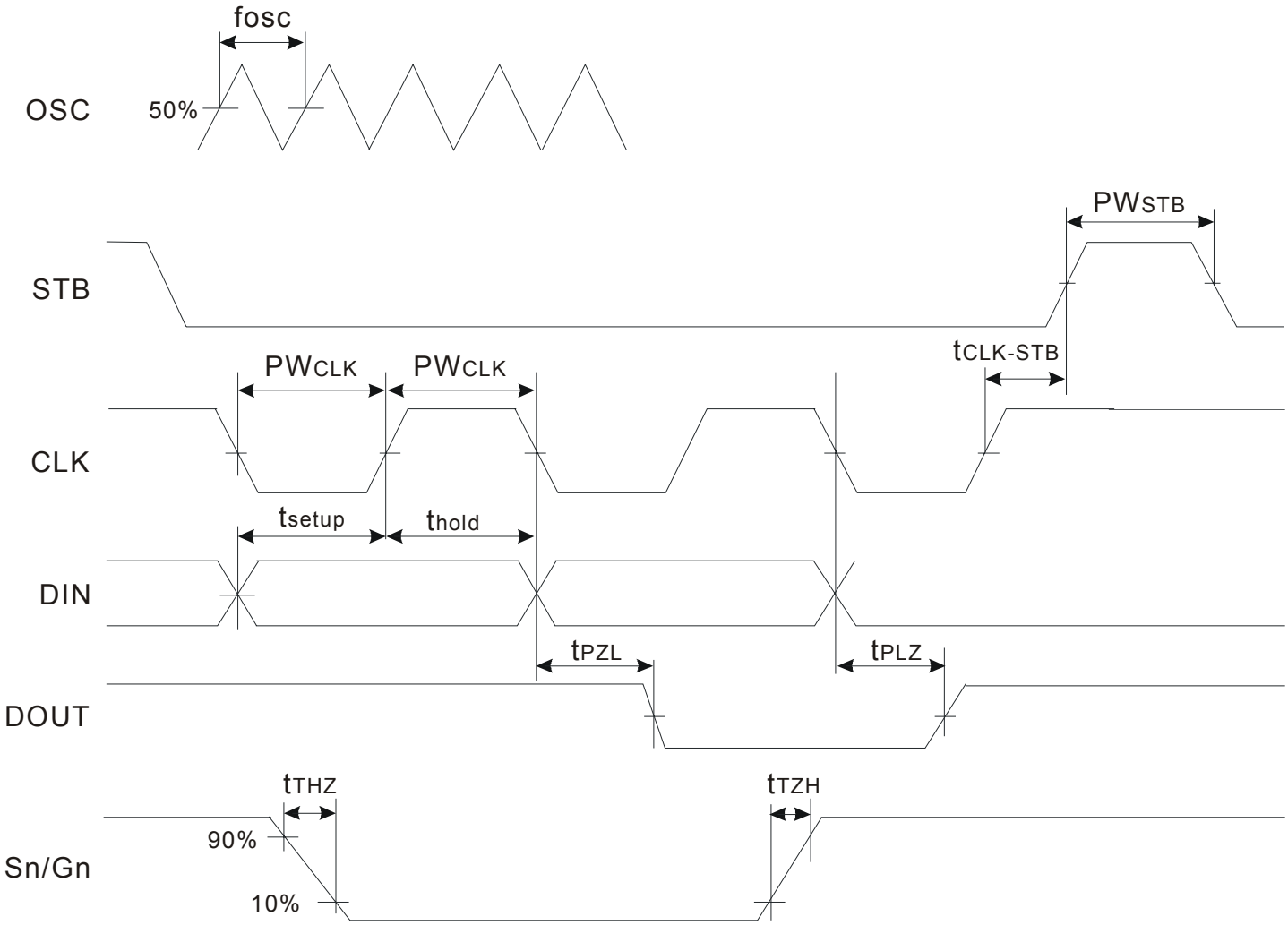
# SWITCHING CHARACTERISTIC WAVEFORM

PT6311 Switching Characteristics Waveform is given below.



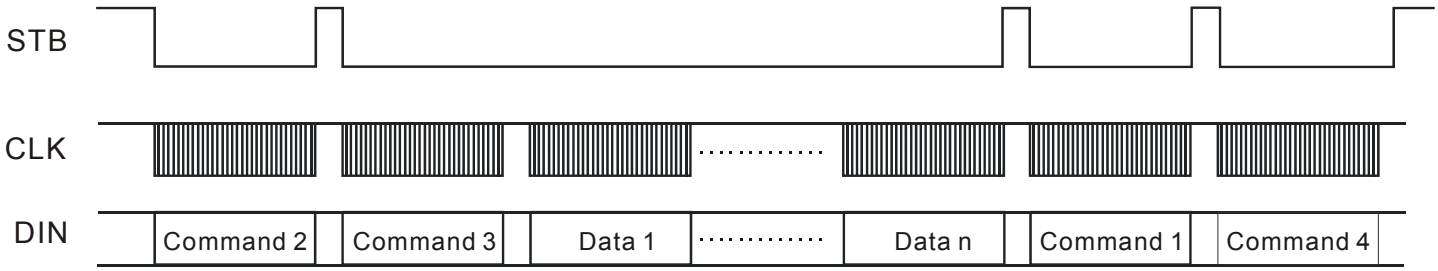

where:

$PW_{CLK}$ (Clock Pulse Width)≥400ns
tsetup (Data Setup Time)≥100ns
$t_{CLK-STB}$ (Clock - Strobe Time)≥1μs
$t_{TZH2}$ (Grid Rise Time)≤0.5μs (VDD=5V)
$t_{TZH2}$ (Grid Rise Time)≤1.2μs (VDD=3.3V)
$t_{TZH1}$ (Segment Rise Time)≤2μs (VDD=5V)
$t_{TZH1}$ (Segment Rise Time)≤4μs (VDD=3.3V)
fosc = Oscillation Frequency

$PW_{STB}$ (Strobe Pulse Width)≥1μs
thold (Data Hold Time)≥100ns
$t_{THZ}$ (Fall Time)≤150μs
$t_{PZL}$ (Propagation Delay Time)≤100ns
$t_{PLZ}$ (Propagation Delay Time)≤400ns (VDD=5V)
$t_{PLZ}$ (Propagation Delay Time)≤600ns (VDD=3.3V)

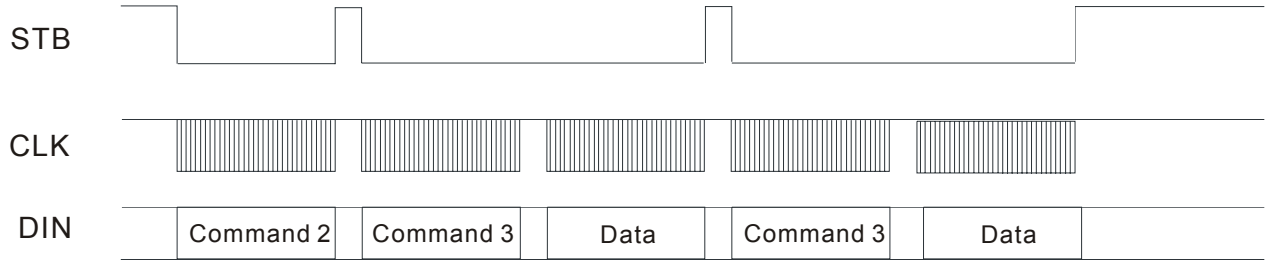
# APPLICATIONS

Display memory are updated by incrementing addresses. Please refer to the following diagram.



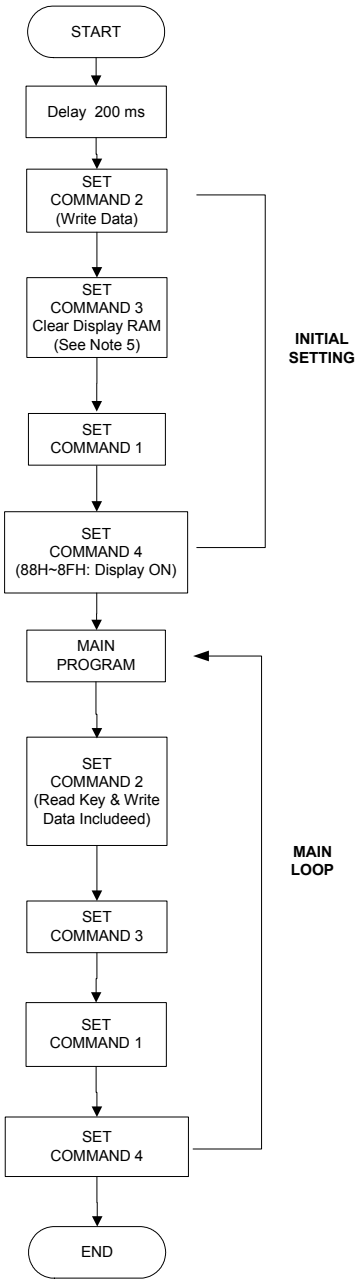

where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (48 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.




where: Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

# RECOMMENDED SOFTWARE FLOWCHART




Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

# ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Logic supply voltage | VDD | -0.3 to +7 | V |
| Driver supply voltage | VEE | VDD +0.3 to VDD -40 | V |
| Logic input voltage | VI | -0.3 to VDD +0.3 | V |
| VFD driver output voltage | VO | VEE -0.3 to VDD +0.3 | V |
| LED driver output current | IOLED | +25 | mA |
| Oscillation frequency | fosc | 3M(Max.) | Hz |
| Operating temperature | Topr | -40 to +85 | ℃ |
| Storage temperature | Tstg | -65 to +150 | ℃ |
| VFD driver output current | IOVFD | -40 (Grid)<br>-15 (Segment) | mA |

# RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=25℃, GND=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Logic supply voltage | VDD | 3 | 5 | 5.5 | V |
| High-Level input voltage | VIH | 0.7VDD | - | VDD | V |
| Low-Level input voltage | VIL | 0 | - | 0.3VDD | V |
| Driver supply voltage | VEE | VDD -35 | - | 0 | V |

# ELECTRICAL CHARACTERISTICS

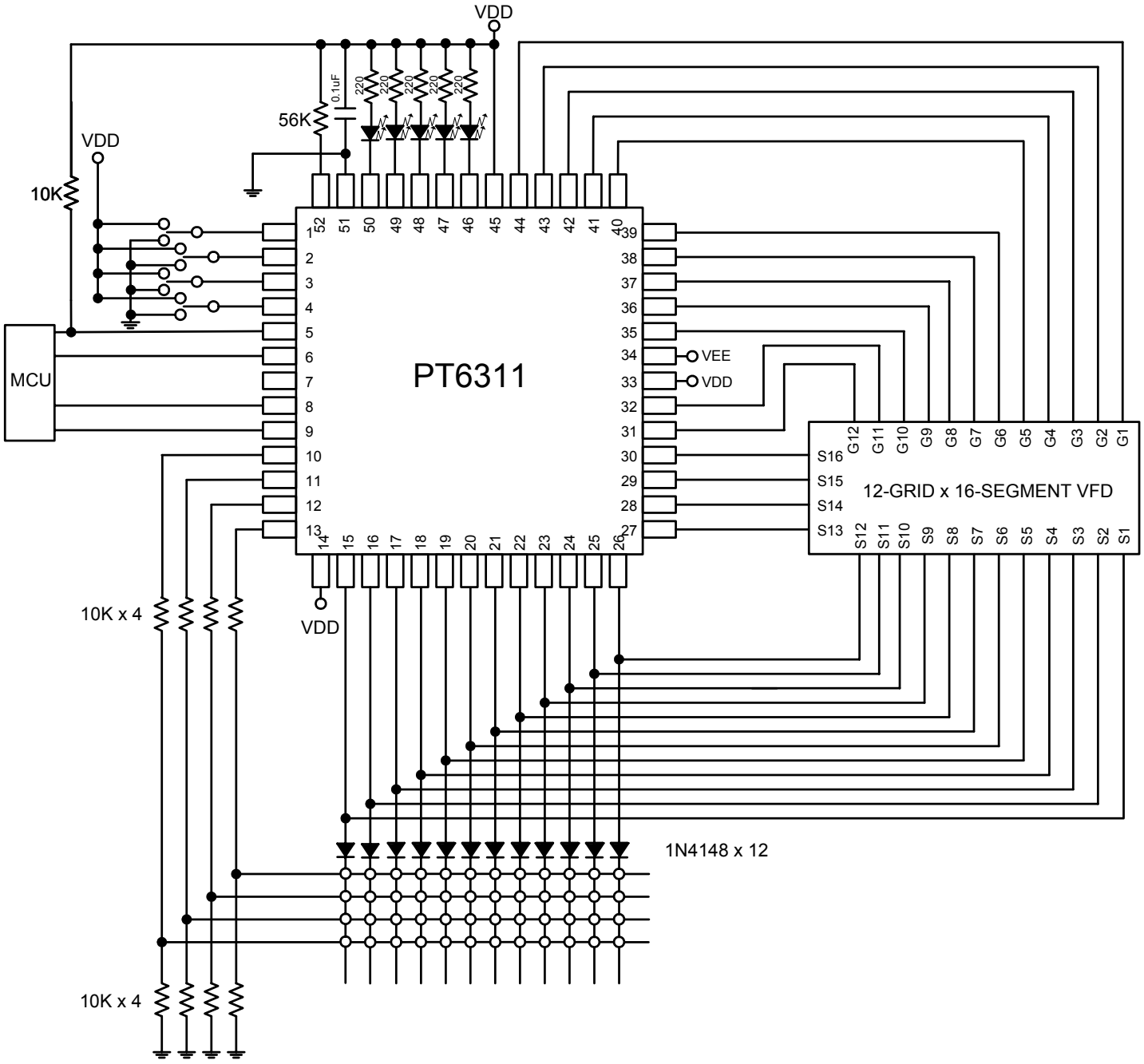
(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35 V, Ta=25℃)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-Level output voltage | VOHLED | IOHLED=-1mA<br>LED1 to LED5 | 0.9VDD | - | - | V |
| Low-Level output voltage | VOLLED | IOLLED=+20mA<br>LED1 to LED5 | - | - | 1 | V |
| Low-Level output voltage | VOLDOUT | DOUT, IOLDOUT=4mA | - | - | 0.4 | V |
| High-Level output current | IOHSG | VO=VDD -2V<br>SG1 to SG12 | -3 | - | - | mA |
| High-Level output current | IOHGR | VO=VDD -2V,<br>GR1 to GR8,<br>SG13/GR16 to SG20/GR9 | -15 | - | - | mA |
| High-Level input voltage | VIH | - | 0.7VDD | - | - | V |
| Low-Level input voltage | VIL | - | - | - | 0.3VDD | V |
| Oscillation frequency | fosc | R=56KΩ | 350 | 500 | 650 | KHz |
| Input current | II | VI=VDD or VSS | - | - | ±1 | μA |
| Dynamic current consumption | IDDdyn | Under no load Display OFF | - | - | 5 | mA |

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35 V, Ta=25℃)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-Level output voltage | VOHLED | IOHLED = -1mA<br>LED1 to LED5 | 0.9VDD | - | - | V |
| Low-Level output voltage | VOLLED | IOLLED = +20mA<br>LED1 to LED5 | - | - | 1 | V |
| Low-Level output voltage | VOLDOUT | DOUT, IOLDOUT = 4mA | - | - | 0.4 | V |
| High-Level output current | IOHSG | VO = VDD -2V<br>SG1 to SG12 | -1.5 | - | - | mA |
| High-Level output current | IOHGR | VO = VDD -2V<br>GR1 to GR8,<br>SG13/GR16 to SG20/GR9 | -6 | - | - | mA |
| High-Level input voltage | VIH | - | 0.7VDD | - | - | V |
| Low-Level input voltage | VIL | - | - | - | 0.2VDD | V |
| Oscillation frequency | fosc | R = 56 KΩ | 350 | 500 | 650 | KHz |
| Input current | II | VI = VDD or VSS | - | - | ±1 | μA |
| Dynamic current consumption | IDDdyn | Under no load Display OFF | - | - | 3 | mA |

# 12-GRID X 16-SEGMENT VFD APPLICATION CIRCUIT



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# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT6311 | 52 Pins, QFP | PT6311 |
| PT6311-LQ | 52 Pins, LQFP | PT6311-LQ |

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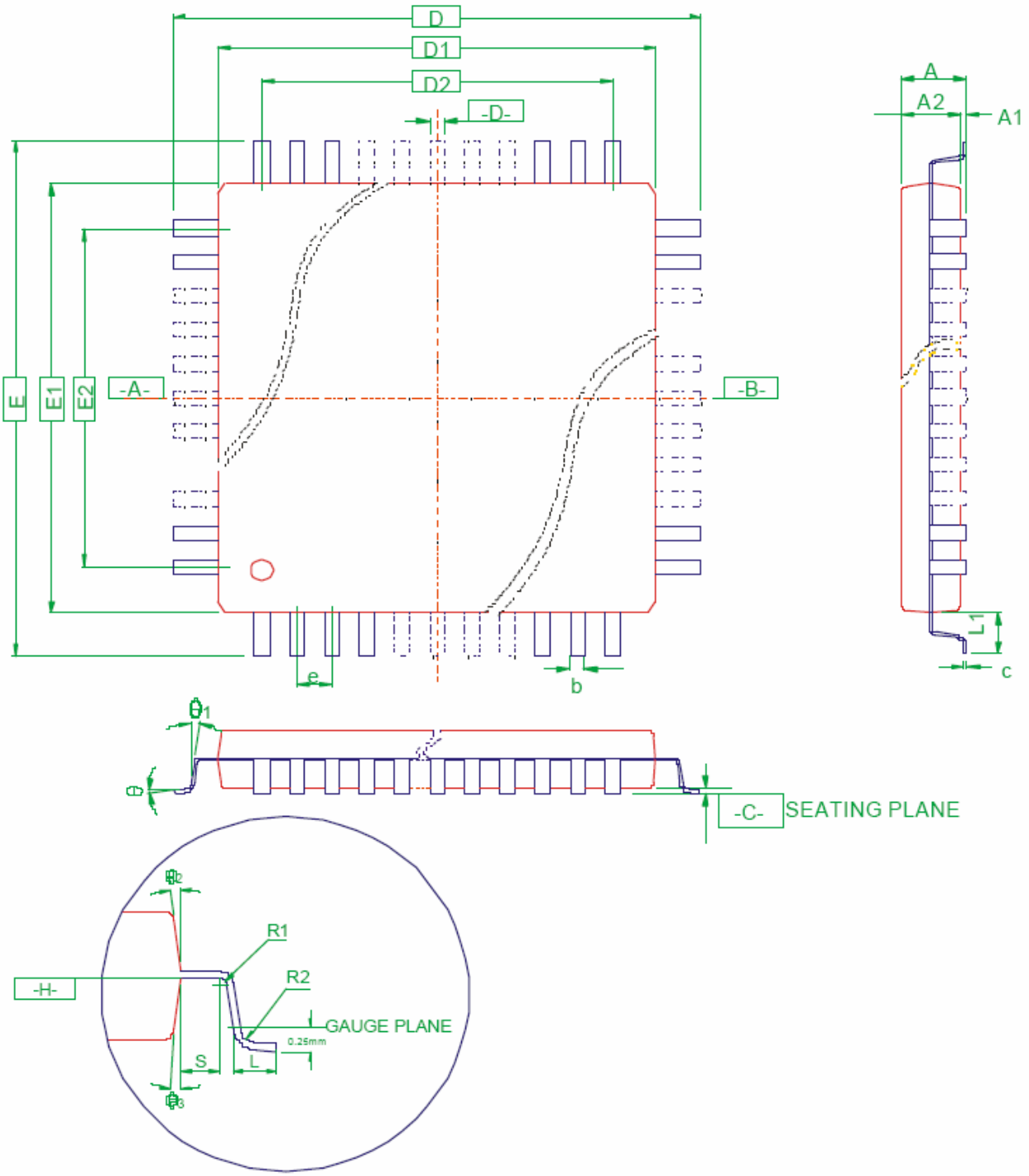
# PACKAGE INFORMATION

## *52 PINS, QFP (BODY SIZE: 14MM X 14MM, PITCH=1.00MM)*



| Symbol | Min. | Nom. | Max |
|---|---|---|---|
| c | 0.11 | - | 0.23 |
| A | - | - | 3.15 |
| A1 | 0.00 | - | 0.25 |
| A2 | 2.50 | 2.70 | 2.90 |
| b | 0.34 | - | 0.50 |
| D | 17.20 BSC. | | |
| D1 | 14.00 BSC. | | |
| D2 | 12.00 REF. | | |
| E | 17.20 BSC. | | |
| E1 | 14.00 BSC. | | |
| E2 | 12.00 REF. | | |
| e | 1.00 BSC. | | |
| L | 0.73 | 0.88 | 1.03 |
| L1 | 1.60 BSC. | | |
| R1 | 0.13 | - | - |
| R2 | 0.13 | - | 0.30 |
| θ | 0° | - | 7° |
| θ1 | 0° | - | - |
| θ2 | 5° | - | 16° |
| θ3 | 5° | - | 16° |
| S | 0.2 | - | - |

Notes:
1. All dimensioning and tolerancing dimension conform to ASME Y14.5M-1994
2. Datum plane “H” is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Datums “A-B” and “D” to be determined at datum plane “H”.
4. To be determine at seating plane “C”.
5. Dimensions “D1” and “E1” do not include mold protrusion, allowable protrusion is 0.25 mm per side, dimensions “D1” and “E1” do include mold mismatch and are determined at datum plane “H”.
6. Details of Pin1 identifier are optional but must be located within the zone indicated.
7. Regardless of the relatie size of the upper and lower body sections, dimensions “D1” and “E1” are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
8. All dimensions are in millimeters.
9. Dimension “b” do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed “b” maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape and size of this feature is optional.
11. N= the number of lead (N=52)
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
13. “A1” is defined as the distance from the seating plane to the lowest point of the package body.
14. Refer to JEDEC MS-022 Variation BD.

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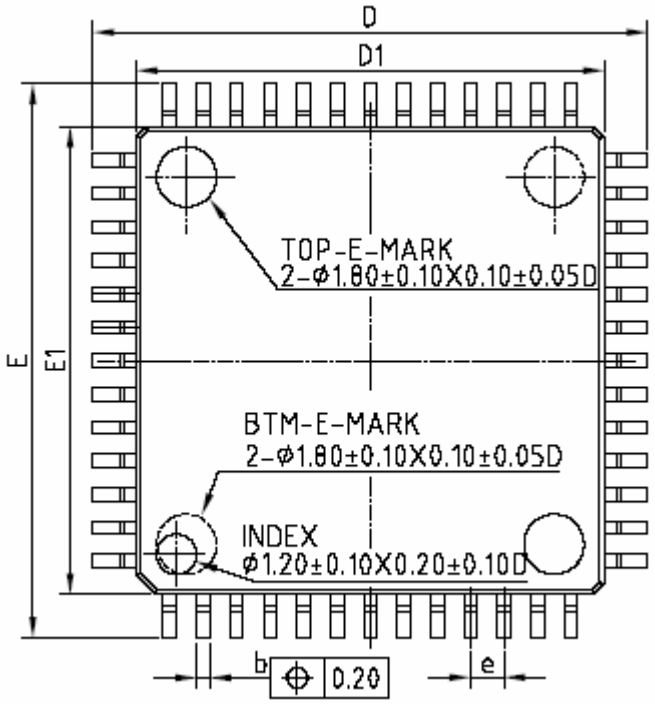
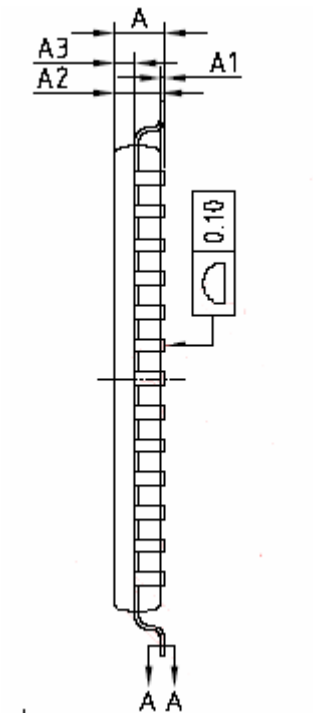
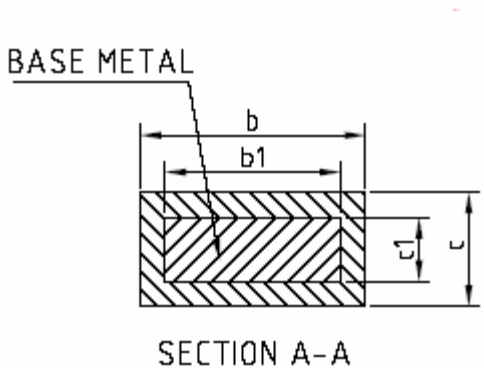
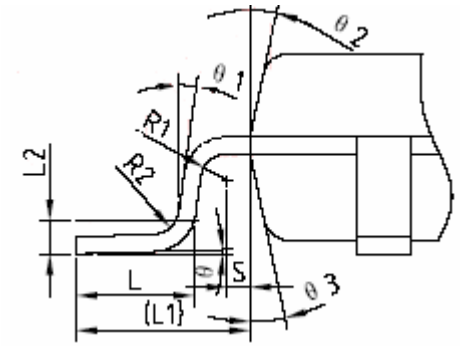
## *52 PINS, LQFP*


D
D1
E
E1
TOP-E-MARK
2-φ1.80±0.10X0.10±0.05D
BTM-E-MARK
2-φ1.80±0.10X0.10±0.05D
INDEX
φ1.20±0.10X0.20±0.10D
b
0.20
e


A
A3
A2
A1
0.10
A A


BASE METAL
b
b1
c1
c
SECTION A-A


θ2
θ1
R1
R2
L2
L
θ
S
θ3
(L1)

| Symbol | Min. | Nom. | Max |
|---|---|---|---|
| A | - | - | 1.6 |
| A1 | 0.05 | - | 0.2 |
| A2 | 1.3 | 1.4 | 1.50 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.36 | - | 0.49 |
| b1 | 0.35 | 0.40 | 0.45 |
| c | 0.13 | - | 0.18 |
| c 1 | 0.12 | 0.13 | 0.14 |
| D | 16.4 | 16.60 | 16.8 |
| D1 | 13.9 | 14.00 | 14.10 |
| E | 16.4 | 16.60 | 16.80 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | 1.00BSC | | |
| L | 0.70 | 0.85 | 1.00 |
| L1 | 1.30REF | | |
| L2 | 0.25BSC | | |
| R1 | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 |
| S | 0.15 | - | - |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | - | - |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. Datums A-B and D to be determined at datum plane H.
3. Dimensions D1 and E1 do not include mold prortrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at the datum plane H.
4. Controlling Dimension: MILLIMETERS
5. Dimension b does not include dambar protrusion. The dambar protrusion (s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot. minimum space between protrusion and as adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Refer to JEDEC MS-026 Variation BCC

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