PLESSEY
Semiconductors

SL701B&C SL702B&C

The SL701B, SL701C, SL702B and SL702C are monolithic, bipolar integrated circuit, high gain D-C amplifiers, intended primarily for use as operational amplifiers or in instrumentation applications. The SL701 basic circuit has an internal zener and provides an output symmetrical about earth using the specified supply voltage. The SL702 basic circuit is non-symmetrical, with a direct output, but may be used with an external zener to permit a symmetrical output to be obtained at the other supply voltages.

The SL701C and SL702C differ from their equivalent devices with suffix B mainly in having higher maximum input offset voltage.

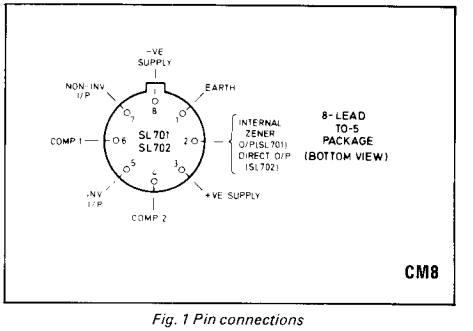


Fig. 1 Pin connections

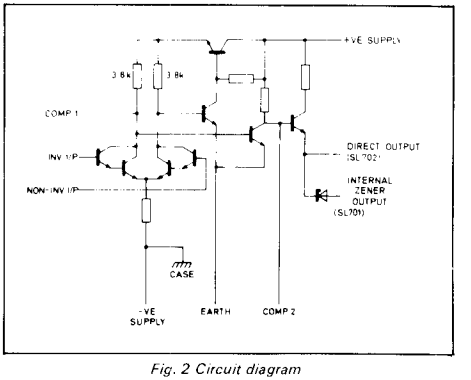


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: (unless otherwise stated)

T_{amb} = +22°C ± 2°C

Supplies = +12V and −12V

A 6.0V zener is added to SL702 except where otherwise stated. (See test circuits)

Characteristic	Circuit	Value			Units	Test conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop gain (Fig. 5)	All	66	70		dB	Frequency = 30kHz	A
Change of gain with temperature	All		±2		dB	Frequency = 20kHz −25°C to +100°C	A

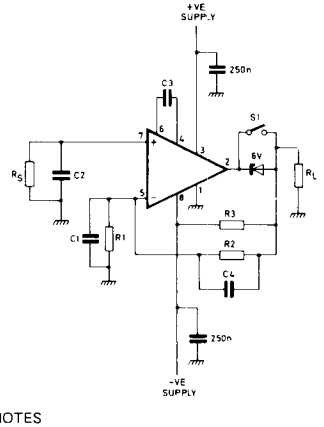
Characteristic	Circuit	Value			Units	Test Conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop bandwidth (Fig. 5)	All	250	500		kHz	High frequency −3dB point	A
Output resistance	All		100		Ω	1kHz	A
Input resistance	All		100		kΩ	1kHz	A
180° phase shift frequency (Fig. 5)	All	20	35		MHz		A
Input offset voltage	SL701B, SL702B			5	mV		1
Input offset voltage	SL701C, SL702C			20	mV		1
Input offset voltage change with temperature	All		15		μV/°C		1
Input current	SL701B, SL702B			1	μA		G & H
Input current	SL701C, SL702C			3	μA		G & H
Input offset current	SL701B, SL702B			0.3	μA		F
Input offset current	SL701C, SL702C			1.8	μA		F
Input offset current change with temperature (see Note)	All		0.4		μA	−25°C to +100°C	F
Common mode rejection ratio (Fig. 4)	SL701B, SL702B	70	80		dB	+0.5V to −3V input square wave	
Common mode rejection ratio (Fig. 4)	SL701C, SL702C	60	80		dB	+0.5V to −3V input square wave	
Supply line rejection	All	60	70		dB	1.0V square wave on supply line	
Positive output clipping level (DC)	All	+3.9	+4.3		V		C
Negative output clipping level (DC)	All	−6.0	−6.5		V		C
Positive output clipping level (DC)	SL702B & C	+ 9.9	+10.3		V	No external zener	C(S1 closed)
Negative output clipping level (DC)	SL702B & C	0	−0.5		V	No external zener	C(S1 closed)
Positive supply line current	All	9.5	12	14.5	mA	Output at 0V (R3 ± 2% tolerance)	A
Negative supply line current	All	7.5	9	10.5	mA	Output at Ov (R3 ± 2% tolerance)	A
Spot noise	All		See Fig. 7			Open loop	

NOTE

Total change in offset current over specified range

Test reference	$R_S(\Omega)$	$R_1(k\Omega)$	$R_2(k\Omega)$	$R_3(k\Omega)$	R_L	$*C_1(\mu F)$	C_2 (nF)	C_3	C_4 (pF)	Remarks
A (Fig. 5 & 10)	50	o/c	100	2.2	o/c	30	o/c	o/c	o/c	Open loop AC gain (Figs. 5 and 10)
B (Fig. 5)	50	o/c	100	2.2	o/c	30	o/c	33pF	o/c	Compensated open loop AC gain (Fig. 5)
C (Fig. 6 & 10)	50	1	99	2.2	o/c	o/c	o/c	33pF	o/c	Gain of 100 (Figs 6 and 10)
D (Fig. 6 & 10)	50	1	9	2.2	o/c	o/c	o/c	33pF	4.7	Gain of 10 (Figs. 6 and 10)
E (Fig. 8)	50	1	99	Varied	Varied	30	o/c	o/c	o/c	Negative swing/load resistance (Fig. 8)
F	100k	o/c	100	2.2	o/c	4	1	1nF	o/c	Input offset current
G	100k	o/c	s/c	2.2	o/c	4	1	1nF	o/c	Input current
H	s/c	o/c	100	2.2	o/c	4	o/c	1nF	o/c	Input current
I	s/c	o/c	s/c	2.2	o/c	4	o/c	1nF	o/c	Input offset voltage

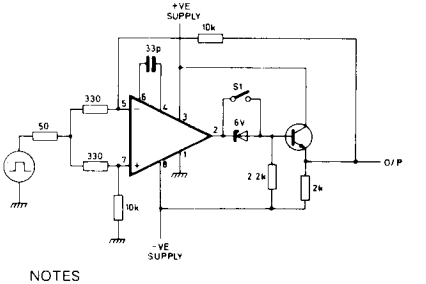
*C_1 should be a non-polarized tantalum or paper type.



NOTES

1. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN EXCEPT WHERE OTHERWISE STATED).

Fig. 3 Test circuit



NOTES

1. THE 330Ω RESISTORS ARE MATCHED TO 0.02% AND THE 10kΩ RESISTORS ARE MATCHED TO 0.05%.
2. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN).

Fig. 4 Common mode test circuit

The test circuit of Fig. 3 is used for measuring all electrical characteristics except common mode rejection. Component values for tests A to I using Fig. 3 are given in the following table.

Frequency Response and Feedback Stabilization

The typical gain/phase frequency response of the device is given in Fig. 5. When the external feedback connections are made the resultant loop gain must be cut at a mean rate of less than 9–10 db/octave. A single dominant time constant is often the simplest solution. For example, in the SL701 and similar amplifiers, a capacitor between pins 5

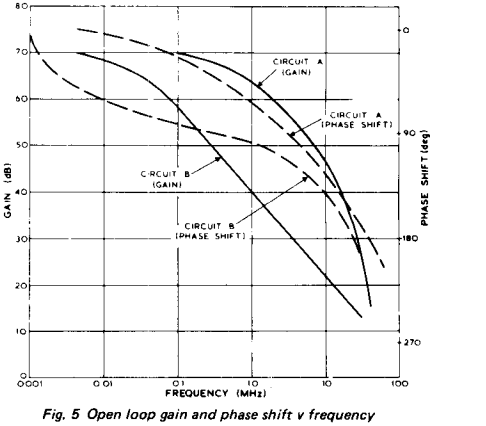


Fig. 5 Open loop gain and phase shift v frequency

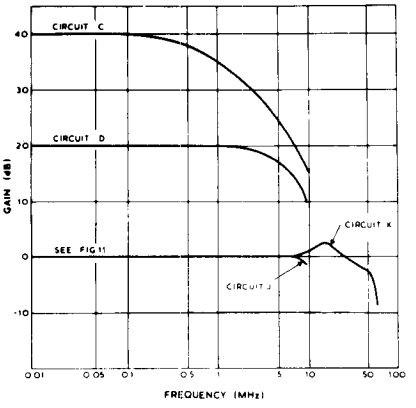


Fig. 6 Gain with feedback v frequency

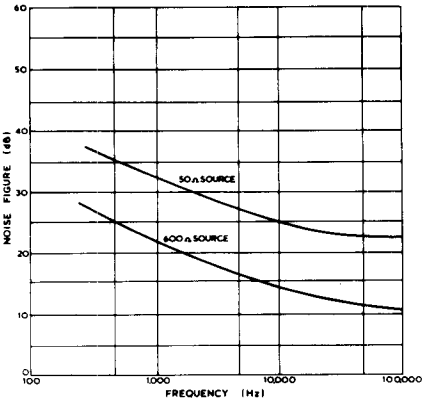


Fig. 7 Spot noise v frequency (open loop)

and 7 with a value between a few tens and a few hundred pF (depending on the feedback fraction) will give a suitable dominant high frequency cut-off. In general, however, when a particular feedback loop is designed, an appropriate stabilizing arrangement, to suit it, will be needed. Except when maximum bandwidth is required, a dominant lag provided by a 33 pF stabilizing capacitor will be found satisfactory for loop gains up to about 20 dB short of the full forward gain of the amplifier; gain curves for this configuration are given in Fig. 6.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage (Fig. 11)	+ 14V and −14V
Output current	20mA

Input voltage (either input, opposite input at 0V) +1V to − 10V.

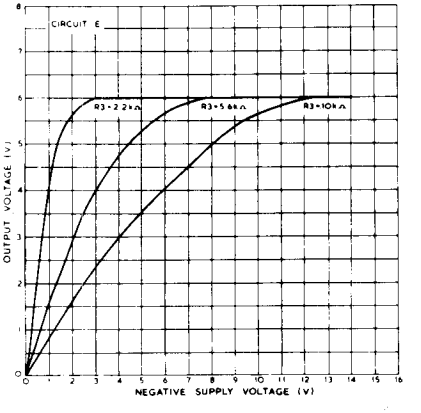


Fig. 8 Max. negative swing as a function of load resistance

Amplifier dissipation at different supply voltages

The curves assume zero load current is drawn from the output. Assuming that a resistor R_3 (zener bias resistor — Fig. 8) is connected between the output and the negative line, the total maximum dissipation will be obtained by adding the power term:

$$\frac{|-V|.|+V|}{R_3}$$

to the value obtained from Fig. 11.

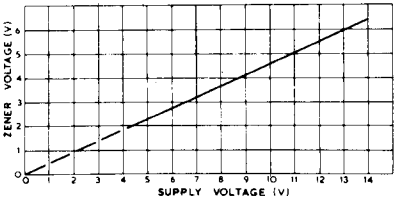


Fig. 9 Zener voltage v supply voltage for symmetrical output about earth

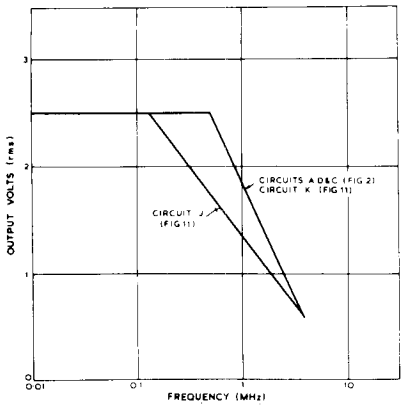


Fig. 10 Typical max. output v frequency

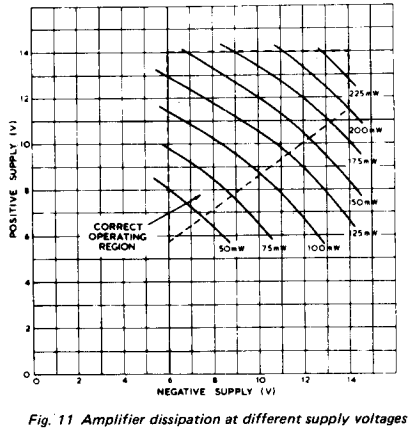


Fig. 11 Amplifier dissipation at different supply voltages

OPERATING NOTES

Lower Supply Voltages (SL702 – with direct output)

The balance of the collector currents of the input transistors is maintained by an auxiliary internal feedback loop, enabling a range of supply voltages to be used, as shown in Fig. 9 and Fig. 11. Since the collector currents of the input transistor are controlled by a 3k Ω 'tail' resistor, the input base current and offset current will decrease and the input resistance will increase as the negative supply rail voltage is reduced. The open loop gain is also affected by this rail voltage and is virtually proportional to it. A reduction in the positive rail voltage does little except decrease various currents and voltages within the circuit; together with the negative supply this decreases the maximum available output level. In order to avoid internal limiting, the magnitude of the positive supply must not be very much lower than that of the negative supply; hence at levels less than the nominal ± 12 volts, attention must be paid to the tolerance of the supplies. Typical characteristics for operation under these conditions are given below.

Test conditions: Supply voltages +6V and −6V
Ambient temperature = +20°C
External zener = 2.7V
Test circuits as above

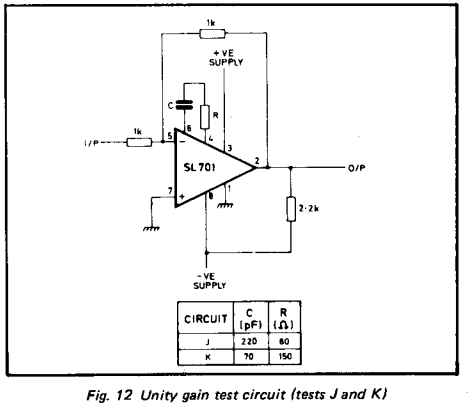


Fig. 12 Unity gain test circuit (tests J and K)

Characteristic	Value	Units	Test conditions
Open loop gain	62	dB	
Input resistance	200	kΩ	
Max. input base current (SL702B) (see note)	500	nA	
Max. input base current (SL702C) (see note)	1.5	μA	
Max. input offset current (SL702B) (see note)	150	nA	
Max. input offset current (SL702C) (see note)	900	nA	
Supply current (+ve)	8	mA	R_3 = 1.2k Ω ± 2%
Supply current (−ve)	6.5	mA	R_3 = 1.2k Ω ± 2%
Output clipping level (+ve)	2	V	
Output clipping level (−ve)	3	V	

NOTE

These figures are not guaranteed, but indicate relation to full specification at ± 12V supplies.

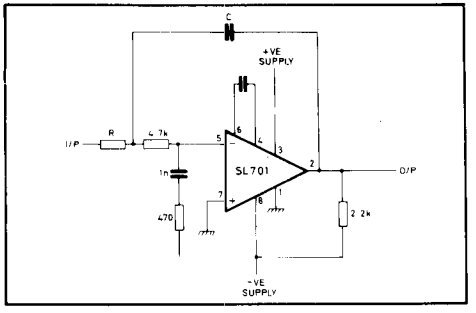


Fig. 13 Integrator circuit

Unity Gain

For unity gain more than one method of compensation may be employed; the simplest is shown in Fig. 12. The disadvantages of the method suggested are that some peculiar overload characteristics may be observed at high frequencies and the maximum signal output without limiting is lower than at higher circuit gains. Circuit K on Fig. 12 gives compensation for wideband response, allowing approximately 1 dB gain rise above the gain at low frequencies. For maximum signal handling, but reduced noise performance, the method as indicated in Fig. 13 may be used.

DEFINITION OF TERMS

Decibel (dB) Units Refers to the conventional expression of a .voltage ratio in logarithmic units, i.e. 20 $\log_{10} V_2/V_1$ dB.

Open Loop Bandwidth The frequency at which the open loop gain falls by 3 dB (factor $\sqrt{2}$) below the value at 1kHz.

Output Resistance The ratio of change in output voltage to the change in output current, measured at the output terminal, under open loop conditions and with zero volts d.c. output level.

Input Resistance The resistance between the input terminals, equivalent at low frequencies to the resistance between input and earth with the other input earthed.

180° Phase Shift Frequency The lowest frequency at which the output phase is shifted 180°, relative to the low frequency value, compared to the input signal under open loop conditions with no compensation capacitors.

Input Offset Voltage The voltage between the input terminals to set the DC output voltage to zero.

Input Current The base current of either input transistor when the DC output voltage is set to zero.

Input Offset Current The difference between the input currents when the output quiescent voltage is zero.

Common mode rejection The ratio between the common mode signal and a differential signal producing the same magnitude of output (dB units).

Supply Line Rejection The ratio between the supply line signal and a differential input producing the same magnitude of output (dB units).

Output Clipping Levels The DC voltage at the output terminal when a voltage of ± 0.1V is applied between the input terminals (Gain x 100, circuit C).